IN THE CLAIMS:

Rewrite the pending claims as follows:

1. (Currently Amended) A controller, comprising:

a first memory interface adapted to be coupled to one or more first memory devices wherein the first memory devices comprise volatile memory devices;

a second memory interface adapted to be coupled to one or more second memory devices wherein the second memory devices comprise non-volatile memory devices; and

interface logic coupled to the first and second interfaces and configured to direct memory transactions having a predefined first characteristic to the first memory interface and to direct at least some memory transactions having a predefined second characteristic to the second memory interface, wherein the second characteristic comprises a usage characteristic selected from the group consisting of a read-mostly characteristic and read-only characteristic; and wherein the usage characteristic of at least some memory transactions is updated during operation.

2. (Cancelled)

3. (Previously presented) The controller of clam 1, wherein the second memory devices have a limited write operation endurance.

4. (Currently Amended) The controller of claim 3, further comprising:

an endurance counter for counting [[the]] a number of write operations to a block of memory cells in the one or more second memory devices.

5. (Original) The controller of claim 3, further comprising:

a set of endurance counters for counting the number of write operations to each block of memory cells in the one or more second memory devices.

6. (Original) The controller of claim 1, further comprising:

a write cache for storing data associated with write operations directed to any of the one or more second memory devices.

7. (Original) The controller of claim 6, wherein the write cache is configured to write data stored therein to the one or more second memory devices when a predefined write cache state occurs.

8. (Original) The controller of claim 6, wherein the controller is configurable to write data stored therein to the one or more second memory devices.

9. (Original) The controller of claim 6, wherein the controller is adapted to relocate one or more pages from the one or more second memory devices to the one or more first memory devices when a predefined write cache state occurs.

10. (Original) The controller of claim 1, wherein the one or more first memory devices are Dynamic Random Access Memory (DRAM) devices and the one or more second memory devices are Flash memory devices.

11. (Currently Amended) The controller of claim 1, further comprising:

a prefetch buffer coupled to the second memory interface and adapted to prefetch data from the one or more second memory devices.

12. (Currently Amended) The controller of claim 11, wherein the second memory interface is configured to reduce power used by the one or more second memory devices between prefetches of data from the one or more second memory devices.

13. (Original) The controller of claim 1, wherein the memory controller is configurable to move pages from the one or more first memory devices to secondary storage and to then power down the one or more first memory devices.

14. (Previously presented) The controller of claim 1, wherein the controller is adapted for use in conjunction with a processor having virtual memory logic for mapping virtual memory addresses into physical memory addresses and page logic for assigning physical memory addresses to virtual memory addresses, wherein the page logic is configured to assign physical memory addresses in the one or more first memory devices to virtual memory addresses associated with a first usage characteristic, and to assign physical memory addresses in the one or more second memory devices to virtual memory addresses associated with a second usage characteristic.

15. (Currently Amended) [[The]] A system, comprising:

a first memory interface adapted to be coupled to one or more first memory devices of a first memory type having a first set of attributes;

a second memory interface adapted to be coupled to one or more second memory devices of a second memory type having a second set of attributes, wherein the first and second sets of attributes have at least one differing attribute;

interface logic coupled to the first and second interfaces and configured to direct memory transactions having a predefined first characteristic to the first memory interface and to direct memory transactions having a predefined second characteristic to the second memory interface; and

a processor having virtual memory logic for mapping virtual memory addresses into physical memory addresses and page logic for assigning physical memory addresses to virtual memory addresses, wherein the page logic is configured to assign physical memory addresses in the one or more first memory devices to virtual memory addresses associated with a first usage characteristic, and to assign physical memory addresses in the one or more second memory devices to virtual memory addresses associated with a second usage characteristic.

16. (Original) The system of claim 15, wherein the first usage characteristic comprises memory usage that includes both read and write operations.

17. (Original) The system of claim 16, wherein the second usage characteristic comprises memory usage that includes only read operations.

18. (Original) The system of claim 16, wherein the second usage characteristic comprises memory usage that includes read operations and less than a threshold amount of write operations.

19. (Original) The system of claim 15, wherein the processor includes a page table cache having entries that include a field whose value is set by the processor in accordance with the first and second usage characteristics.

20. (Original) The system of claim 15, including a page table, for mapping virtual memory pages to physical memory pages, having a plurality of entries that include a field whose value is set in accordance with whether corresponding virtual memory pages are associated with the first or second usage characteristic.

21. (Original) The system of claim 20, wherein the system is configured to change the value of the field in an entry of the page table based on usage of the corresponding page.

22. (Original) A method of managing memory in a non-homogeneous memory system, comprising:

establishing a plurality of page table entries, each entry in the plurality of page table entries mapping a virtual memory page address to a physical memory page address, each said entry including a usage field identifying a respective portion of main memory in which the physical memory page address is located, wherein the main memory includes at least two distinct portions, including a first portion implemented with one or more first memory devices of a first memory type having a first set of attributes and a second portion implemented with one or more second memory devices of a second memory type having a second set of attributes, wherein the first and second sets of attributes have at least one differing attribute;

receiving a memory transaction request;

translating a virtual address of a page associated with the memory transaction request into a physical address in accordance with a corresponding page table entry of the plurality of page table entries, the physical address comprising a physical address in a respective portion of main memory;

directing the memory transaction to the physical address in the respective portion of main memory.

23. (Previously presented) The method of claim 22, wherein the first memory devices are volatile memory devices, the first set of attributes include an unlimited endurance characteristic, the second memory devices are non-volatile memory devices, and the second set of attributes include a limited endurance characteristic.

24. (Original) The method of claim 22, wherein the second memory devices are non-volatile memory devices and the first memory devices are volatile memory devices.

25. (Original) The method of claim 22, further comprising:

determining if an endurance limitation associated with one of the second memory devices has been exceeded; and

redirecting the memory transaction if the endurance limitation not been exceeded.

26. (Original) The method of claim 22, wherein the second memory devices are non-volatile memory devices, and the method includes:

redirecting at least one write operation directed to one of the second memory devices to a write cache.

27. (Original) The method of claim 26, further comprising:

determining if the write cache can accept a write operation; and

writing the page to the write cache if the write cache can accept a write operation.

28. (Original) The method of claim 22, wherein the second memory devices are non-volatile memory devices and the method includes:

pre-fetching data from the second memory device.

29. (Original) The method of claim 28, including reducing power to the one or more second memory devices between prefetches.

30. (Original) The method of claim 22, including moving pages from the one or more first memory devices to secondary storage and then powering down the one or more first memory devices.

31. (Currently Amended) A controller, comprising:

first interface means for coupling the controller to one or more first memory devices wherein the first memory devices comprise volatile memory devices;

second interface means for coupling the controller to one or more second memory devices wherein the second memory devices comprise non-volatile memory devices; and

logic means coupled to the first and second interface means for directing memory transactions having a predefined first characteristic to the first memory interface means and for directing at least some memory transactions having a predefined second characteristic to the second memory interface means, wherein the second characteristic comprises a usage characteristic selected from the group consisting of a read-mostly characteristic and read-only characteristic; and wherein the usage characteristic of at least some memory transactions is updated during operation.

32. (Currently Amended) [[The]] A system, comprising:

first interface means for coupling to one or more first memory devices of a first memory type having a first set of attributes;

second interface means for coupling to one or more second memory devices of a second memory type having a second set of attributes, wherein the first and second sets of attributes have at least one differing attribute;

logic means coupled to the first and second interface means for directing memory transactions having a predefined first characteristic to the first ~~memory~~ interface means and to direct memory transactions having a predefined second characteristic to the second ~~memory~~ interface means; and

virtual memory means for mapping virtual memory addresses into physical memory addresses and page means for assigning physical memory addresses to virtual memory addresses, wherein the page means assigned physical memory addresses in the one or more first memory devices to virtual memory addresses associated with a first usage characteristic, and assigns physical memory addresses in the one or more second memory devices to virtual memory addresses associated with a second usage characteristic.